REMARKS

Reconsideration of the application, in view of the above amendments and following remarks is respectfully requested.

The Examiner continues to reject Claims 12 and 15-21 under 35 U.S.C. §102(e) as being anticipated by Kelly et al. The Examiner states that the Applicant's amendment filed on May 29, 2007 has been fully considered but does not place the application in condition for allowance. The Examiner states that in Applicant's argument that Kelly does not disclose a head pointer stored in a common memory through a plurality of ports, the Examiner respectfully disagrees. The Examiner points to Kelly at Column 9, Lines 35-64, Column 4, Lines 50-65 to show that an output buffer is a common memory which included the selected package, which included data portion and head pointer for each transaction. The Examiner stated that each transaction is represented in each packet which contained information required to determine the characteristics and purpose of each transaction which is the address and data information. The Examiner states that the prior art thus teaches the invention as claimed and the amended claims do not distinguish over the prior art as applied.

This rejection is respectfully traversed in Paragraph 2 of the official action, the Examiner refers to Column 8, Lines 40-65 of Kelly et al. Referring now specifically to the sentence beginning on Line 62, which we cite:

> "Only a single input buffer set 831 is provided for handling traffic, per virtual channel, in the downstream path from the upstream port. Separate single input buffer sets 839 and 841 are provided at each of the downstream ports, per virtual channel for handling traffic in the upstream direction." (emphasis added)

Therefore, it is clear that Kelly et al functions in terms of the prior art by requiring separate memories for the input port and for each of the two output ports. Furthermore, each of these memories has a separate buffer per virtual channel. As is well known to those skilled in the arts PCI Express supports eight virtual channels. Thus, in Kelly there would be a minimum of 24 separate memories in the configuration discussed in Figure 8 whereas only a single memory required in the present invention. In the present

invention, the single memory is shared between the three ports that make up a minimal PCI Express switch by storing the head pointer at the port and some additional characterization information, but not storing the data at the port, as in Kelly et al.

As to the term "head pointer", the Examiner is confusing this with the term of "header" referred to in the portion of Column 4, Lines 50-65, recited by the Examiner. If you review the text in this section carefully, the only term that is used is "header" not "head pointer". The term "header" is defined in the PCI Express base specification, revision 1.0(a) as a set of fields that appear in front of a Packet that contain the information required to determine the characteristics and purpose of the Packet. We have taken the definition for the term "head pointer" from the United States Patent 7,124,241 which recites: The "head" pointer that defines the memory address where the Packet should first begin to be written into the memory banks. Also in United States Patent 4,543,626 it recites that in one embodiment, the work queued is located in the control memory (22) and defined by a head pointer (60) which points to or contains the address of the location in control memory containing the first control block in the stations work cue (58,…). For the Examiner's convenience, a copy of the specific portion of the patents reciting these definitions is attached hereto. Accordingly, the "head pointer" points to the head or beginning of the file or in this case the Packet when it is stored in the memory. This is not at all equivalent to the "header" referred to in the Kelly et al patent, the Examiner's statement to the contrary notwithstanding.

As stated in the background of the invention portion of the present application, for a given number of Packets that need to be stored, the amount of memory space in the buffer memory [such as in Kelly et al] must be N times to the equivalent of the switch's sum total of credits, where N is the number of ports of the switch, because all the data from all ingress ports could go to a single egress for each egress port. As is well known to those skilled in the art, increasing the memory size not only increases the cost of the integrated circuit, but the size thereof which and reduces the yields from the manufacturing process further increasing the cost; and increasing the complexity of the chip as well as the size of the resulting PCI Express switch.

Accordingly, the present invention overcomes the problems in the prior art, such as Kelly et al. Therefore, the Examiner's 102 objection should be withdrawn.

In order to clarify this for the Examiner, Claim 12 has been amended in order to recite that the data is stored in a single common memory shared by a plurality of ports and a the wherein clause has been added that duplication of memory at the plurality of ports is eliminated. This feature is not shown or suggested by Kelly et al.

Accordingly, Applicants believe that the application, as amended, is in condition for allowance and such action is respectfully requested.

Respectfully submitted,
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